In re Patent Application of
BERTRAND ET AL.
Serial No. **10/813,564**
Filed: **MARCH 30, 2004**

In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-11 (canceled).

12. (Currently amended) A comparator with two thresholds comprising:

a two-threshold latch including an input and an output respectively forming an input and an output of the comparator, and including a first node between a first power supply terminal and the output of the comparator; and

a first negative feedback loop acting on the first node for setting a first threshold of the comparator as a function of a first power supply potential applied to the first power supply terminal, and as a function of a first reference potential;

wherein the first threshold is an upper threshold, and the first reference potential is less than or equal to the first power supply potential, which is positive, and wherein ~~the first threshold is set so that~~ a difference between the first power supply potential and the first reference potential is positive and increases as a function of the first power supply potential to limit an increase in the first threshold when the first power supply potential increases.

13. (Previously presented) A comparator according to Claim 12, wherein said two-threshold latch further includes

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PAGE 4/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

a second node between a second power supply terminal and the output of the comparator; and further comprising a second negative feedback loop for setting a second threshold of the comparator as a function of a second power supply potential applied to the second power supply terminal, and as a function of a second reference potential.

14. (Canceled).

15. (Canceled).

16. (Previously presented) A comparator according to Claim 12, wherein the second threshold is a lower threshold, and the second reference potential is greater than or equal to the second power supply potential, which is ground.

17. (Previously presented) A comparator according to Claim 12, wherein said first negative feedback loop comprises first and second transistors each comprising a source, a drain and a gate, with the source of said first transistor being connected to the first node, the gate of said first transistor being connected to the source of said second transistor, the gate of said second transistor being connected to the output of the comparator, the first power supply potential being applied to the drain of said first transistor, and the first reference potential being applied to the drain of said second transistor.

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PAGE 5/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

In re Patent Application of
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18. (Previously presented) A comparator according to Claim 17, wherein said first negative feedback loop further comprises a third transistor comprising a drain connected to the gate of said first transistor, a gate connected to the output of the comparator, and a source connected to the second power supply potential.

19. (Previously presented) A comparator according to Claim 14, wherein said second negative feedback loop comprises fourth and fifth transistors each comprising a source, a drain and a gate, with the source of said fourth transistor being connected to the second node, the gate of said fourth transistor being connected to the source of said fifth transistor, the gate of said fifth transistor being connected to the output of the comparator, the second power supply potential being applied to the drain of said fourth transistor, and the second reference potential being applied to the drain of said fifth transistor.

20. (Previously presented) A comparator according to Claim 19, wherein said second negative feedback loop further comprises a sixth transistor comprising a drain connected to the gate of said fourth transistor, a gate connected to the output of the comparator, and a source connected to the first power supply potential.

BEST AVAILABLE COPY

PAGE 6/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

In re Patent Application of
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Serial No. **10/813,564**
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21. (Previously presented) A comparator according to Claim 12, wherein said two-threshold latch comprises a plurality of transistors series-connected between the first power supply terminal and a second power supply terminal, said plurality of transistors each comprising a gate connected together and to the input of said two-threshold latch, said plurality of transistors including seventh and eight transistors having a first type of conductivity, and ninth and tenth transistors having a second type of conductivity.

22. (Previously presented) A comparator according to Claim 21, wherein said eight and ninth transistors each comprises a drain connected together; and wherein said two-threshold latch further comprises an inverter connected between the drain of said eighth and ninth transistors and the output of the comparator.

23. (Currently amended) A comparator comprising:

a latch connected between first and second power supply terminals and having an upper threshold and a lower threshold, said latch including an input and an output respectively forming an input and an output of the comparator, a first node between the first power supply terminal and the output of the comparator, and a second node between the second power supply terminal and the output of the comparator;

a first negative feedback loop acting on the first node for setting a first threshold of the comparator as a function of a first power supply potential applied to the

BEST AVAILABLE COPY

PAGE 7/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

first power supply terminal, and as a function of a first reference potential applied to said first negative feedback loop; and

a second negative feedback loop for setting a second threshold of the comparator as a function of a second power supply potential applied to the second power supply terminal, and as a function of a second reference potential applied to said second negative feedback loop;

wherein the first threshold is an upper threshold, and the first reference potential is less than or equal to the first power supply potential, which is positive, and wherein ~~the first threshold is set so that~~ a difference between the first power supply potential and the first reference potential is positive and increases as a function of the first power supply potential to limit an increase in the first threshold when the first power supply potential increases.

24. (Canceled).

25. (Canceled).

26. (Previously presented) A comparator according to Claim 23, wherein the second threshold is a lower threshold, and the second reference potential is greater than or equal to the second power supply potential, which is ground.

BEST AVAILABLE COPY

In re Patent Application of
BERTRAND ET AL.
Serial No. **10/813,564**
Filed: **MARCH 30, 2004**

27. (Previously presented) A comparator according to Claim 23, wherein said first negative feedback loop comprises first and second transistors each comprising a source, a drain and a gate, with the source of said first transistor being connected to the first node, the gate of said first transistor being connected to the source of said second transistor, the gate of said second transistor being connected to the output of the comparator, the first power supply potential being applied to the drain of said first transistor, and the first reference potential being applied to the drain of said second transistor.

28. (Previously presented) A comparator according to Claim 27, wherein said first negative feedback loop further comprises a third transistor comprising a drain connected to the gate of said first transistor, a gate connected to the output of the comparator, and a source connected to the second power supply potential.

29. (Previously presented) A comparator according to Claim 23, wherein said second negative feedback loop comprises fourth and fifth transistors each comprising a source, a drain and a gate, with the source of said fourth transistor being connected to the second node, the gate of said fourth transistor being connected to the source of said fifth transistor, the gate of said fifth transistor being connected to the output of the comparator, the second power supply potential being applied to the drain of said fourth

BEST AVAILABLE COPY

PAGE 9/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

transistor, and the second reference potential being applied to the drain of said fifth transistor.

30. (Previously presented) A comparator according to Claim 29, wherein said second negative feedback loop further comprises a sixth transistor comprising a drain connected to the gate of said fourth transistor, a gate connected to the output of the comparator, and a source connected to the first power supply potential.

31. (Previously presented) A comparator according to Claim 23, wherein said latch comprises a plurality of transistors series-connected between the first power supply terminal and the second power supply terminal, said plurality of transistors each comprising a gate connected together and to the input of said latch, said plurality of transistors including seventh and eight transistors having a first type of conductivity, and ninth and tenth transistors having a second type of conductivity.

32. (Previously presented) A comparator according to Claim 31, wherein said eight and ninth transistors each comprises a drain connected together; and wherein said latch further comprises an inverter connected between the drain of said eighth and ninth transistors and the output of the comparator.

BEST AVAILABLE COPY

PAGE 10/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

In re Patent Application of
BERTRAND ET AL.
Serial No. **10/813,564**
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33. (Currently amended) A method for setting upper and lower thresholds of a comparator comprising a latch connected between first and second power supply terminals, the latch including an input and an output respectively forming an input and an output of the comparator, a first node between the first power supply terminal and the output of the comparator, and a second node between the second power supply terminal and the output of the comparator, the method comprising:

forming a first negative feedback loop acting on the first node for setting the upper threshold of the comparator as a function of a first power supply potential applied to the first power supply terminal, and as a function of a first reference potential applied to the first negative feedback loop; and

forming a second negative feedback loop for setting the lower threshold of the comparator as a function of a second power supply potential applied to the second power supply terminal, and as a function of a second reference potential applied to the second negative feedback loop;

wherein the first reference potential is less than or equal to the first power supply potential, which is positive, and wherein ~~the first threshold is set so that~~ a difference between the first power supply potential and the first reference potential is positive and increases as a function of the first power supply potential to limit an increase in the first threshold when the first power supply potential increases.

BEST AVAILABLE COPY

PAGE 11/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

In re Patent Application of
BERTRAND ET AL.
Serial No. **10/813,564**
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34. (Canceled).

35. (Canceled).

36. (Previously presented) A method according to Claim 33, wherein the second reference potential is greater than or equal to the second power supply potential, which is ground.

37. (Previously presented) A method according to Claim 33, wherein the first negative feedback loop comprises first and second transistors each comprising a source, a drain and a gate, with the source of the first transistor being connected to the first node, the gate of the first transistor being connected to the source of the second transistor, the gate of the second transistor being connected to the output of the comparator, the first power supply potential being applied to the drain of the first transistor, and the first reference potential being applied to the drain of the second transistor.

38. (Previously presented) A method according to Claim 37, wherein the first negative feedback loop further comprises a third transistor comprising a drain connected to the gate of the first transistor, a gate connected to the output of the comparator, and a source connected to the second power supply potential.

BEST AVAILABLE COPY

PAGE 12/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58

39. (Previously presented) A method according to Claim 33, wherein the second negative feedback loop comprises fourth and fifth transistors each comprising a source, a drain and a gate, with the source of the fourth transistor being connected to the second node, the gate of the fourth transistor being connected to the source of the fifth transistor, the gate of the fifth transistor being connected to the output of the comparator, the second power supply potential being applied to the drain of the fourth transistor, and the second reference potential being applied to the drain of the fifth transistor.

40. (Previously presented) A method according to Claim 39, wherein the second negative feedback loop further comprises a sixth transistor comprising a drain connected to the gate of the fourth transistor, a gate connected to the output of the comparator, and a source connected to the first power supply potential.

41. (Previously presented) A method according to Claim 33, wherein the latch comprises a plurality of transistors series-connected between the first power supply terminal and the second power supply terminal, the plurality of transistors each comprising a gate connected together and to the input of the latch, the plurality of transistors including seventh and eight transistors having a first type of conductivity, and ninth and tenth transistors having a second type of conductivity.

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In re Patent Application of
BERTRAND ET AL.
Serial No. **10/813,564**
Filed: **MARCH 30, 2004**

42. (Previously presented) A method according to Claim 41, wherein the eight and ninth transistors each comprises a drain connected together; and wherein the latch further comprises an inverter connected between the drain of said eighth and ninth transistors and the output of the comparator.

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PAGE 14/20 * RCVD AT 4/10/2006 4:44:00 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/6 * DNIS:2738300 * CSID: * DURATION (mm-ss):04-58